What is claimed is:

1. A memory circuit for temporarily storing information symbols to receive a signal according to a CDMA system which allows multi-code communication and carry out coherent detection using a pilot symbol, comprising:

a plurality of electrically independent memory blocks, each memory block corresponding to each code in said multi-code communication; and

a memory interface section that carries out data write and data read on each of said plurality of blocks periodically while controlling access timing so that write access and read access to one memory block do not occur simultaneously.

2. A memory circuit for temporarily storing a predetermined number of information symbols to receive a signal according to a CDMA system which allows multi-code communication and carry out coherent detection using a pilot symbol, comprising:

a plurality of electrically independent memory blocks, each memory block corresponding to one code in said multi-code communication and one slot of the reception signal; and

a memory interface section that carries out data write and data read on each of said plurality of blocks periodically while controlling access timing so that write access and read access to one memory block do not occur simultaneously.

3. The memory circuit according to claim 2, wherein said memory interface section selectively accesses a memory block corresponding to a slot subject to coherent detection and a memory block corresponding to a slot currently being received.

4. A memory circuit for temporarily storing a predetermined number of information symbols to receive a signal according to a CDMA system which allows multi-code communication and carry out coherent detection using a pilot symbol, comprising:

a plurality of electrically independent memory blocks, each memory block corresponding to one code in said multi-code communication and one slot of the reception signal;

a memory interface section that carries out data write and data read on each of said plurality of blocks periodically while controlling access timing so that write access and read access to one memory block do not occur simultaneously; and

a memory operation control section that sets memory blocks to which no access is generated to a low power consumption mode.

5. The memory circuit according to claim 4, wherein the low power consumption mode of said memory blocks is implemented by stopping the supply of an operating clock.

6. A coherent detection circuit using a pilot symbol that carries out coherent detection by estimating phase variations using known pilot symbols periodically

inserted in information symbols and compensating for the phases of information symbols, comprising:

an information symbol storage memory circuit having a plurality of electrically independent memory blocks, each memory block corresponding to one code and one slot of the reception signal in said multi-code communication; and;

a phase estimation section that carries out phase estimations of pilot symbols using a plurality of pilot symbols located near a slot to be detected;

an interpolation section that determines the phases of information symbols based on the estimation result of said phase estimation section;

a coherent detection section that carries out coherent detection at timing that matches the phases of said information symbols corrected by said interpolation section; and

a memory operation control section that controls the respective operating modes of said plurality of memory blocks of said information symbol storage memory based on multi-code information and slot information and sets memory blocks to which no access is generated to a low power consumption mode.

7. The coherent detection circuit using a pilot symbol according to claim 6, wherein the low power consumption mode of said memory blocks is implemented by stopping the supply of an operating clock.

8. The coherent detection circuit using a pilot symbol

according to claim 6, further comprising a memory interface section that controls data write to said symbol storage memory, wherein said memory interface section receives despread data of a plurality of delayed signals corresponding to the respective codes output from a plurality of RAKE fingers and writes data to said symbol storage memory on a time-division basis.

9. A CDMA receiver comprising:

a reception antenna;

a high frequency signal processing section that carries out filtering at a predetermined frequency and demodulation to a baseband signal;

an A/D conversion section that converts an analog signal to a digital signal;

a despreading section that despreads the reception signal at predetermined timing and demodulates the data;

the coherent detection circuit using a pilot symbol according to claim 6 that carries out coherent detection on the despread data;

a RAKE combining section that RAKE-combines the despread and coherent-detected multi-paths; and

a channel CODEC section that carries out channel decoding.

10. An information symbol storage memory access control method, comprising the steps of:

providing an information symbol storage memory whose memory area is divided into a plurality of electrically independent memory blocks based on at least

one of information on the number of multi-codes and slot information; and

carrying out data write and data read on each of said plurality of blocks periodically while controlling access timing so that write access and read access to one memory block do not occur simultaneously.

11. An information symbol storage memory access control method, comprising the steps of:

providing an information symbol storage memory whose memory area is divided into a plurality of electrically independent memory blocks based on at least one of information on the number of multi-codes and slot information;

carrying out data write and data read on each of said plurality of blocks periodically while controlling access timing so that write access and read access to one memory block do not occur simultaneously; and

setting said blocks that are subject to neither data write nor data read to a low power consumption mode.

12. The information symbol storage memory access control method according to claim 11, wherein the low power consumption mode of said blocks is implemented by stopping the supply of an operating clock.